

Application for United States Letters Patent  
for  
**Combined Pre-Equalizer and Nyquist Filter**  
by  
Xiaoshu Qian  
David H. Tran  
and  
Ahmed M. Said

Seth Z. Kalson  
Intel Corp

## Field

Embodiments of the present invention relate to digital signal processing, and more particularly, digital signal processing for a cable modem.

## Background

5       Cable modems allow for communicating via CATV (Community Access Television) coaxial cable. Specifications for cable modems are published under the auspices of Cable Television Laboratories, also known as CableLabs®, www.cablelabs.com, a non-profit research and development consortium of cable system operators. Fig. 1 illustrates a functional block diagram for the physical layer of a prior art  
10      cable modem according to DOCSIS (Data Over Cable Service Interface Specification), see CableLabs.

In Fig. 1, block framer **102** frames digital data, and provides these frames to Reed-Solomon encoder **104**. Randomizer **106** reduces any constant component (e.g., a string of zeros) in the output of Reed-Solomon encoder **104**. Preamble **108** provides a  
15      training sequence, used by a receiver at the head end (not shown) for TDMA (Time Division Multiple Access) communication. Symbol map **110** maps digital data to a symbol chosen from a 16QAM (Quadrature Amplitude Modulation) signal constellation. Each of these symbols may be represented by 2 bits for the I (In-phase) component and 2  
20      bits for the Q (Quadrature) component. Nyquist filter **112** filters the digital output from symbol map **110** so as to reduce ISI (Inter-Symbol Interference). Modulator **114** up-converts the digital signal, and digital-to-analog **116** converts the digital signal to an analog signal. Cable interface **118** provides the proper interface to cable **120**.

Nyquist filter **112** is a real-valued digital filter. Nyquist filter **112** provides interpolation, so that the time spacing of a discrete-time signal at the output of Nyquist  
25      filter **112** is less than the time spacing of a discrete-time signal at its input. An embodiment of Nyquist filter **112** is illustrated in Fig. 2, where Nyquist filter **112** is implemented as a FIR (Finite Impulse Response) filter, and the interpolation is such that if the time spacing of a discrete-time signal to the input of Nyquist filter **112** is denoted by  $T$ , then the time spacing of a discrete-time signal at its output is  $T/4$ . The filter of Fig.  
30      2 is implemented as a tap delay line, with unit delay elements **202**. The filter tap weights are denoted by  $c(i), i = 0, 1, \dots, N - 1$ , where  $N$  is the filter length. Adder unit **202** adds

the weighted results to provide the filtered output. Interpolation element 206 indicates that three zeroes are inserted for each input date symbol. In practice, there would be one filter for the in-phase component and one filter for the quadrature component, but for simplicity, only one filter is illustrated in Fig. 2.

5 A change to the cable modem standard DOCSIS (Radio Frequency Interface Specification, SP-RFIv1.1-I02-990731) requires that a transmit pre-equalizer be supported in a cable modem at subscriber locations. The output of Nyquist filter 112 for some embodiments is 10 bits, and consequently applying a pre-equalizer to the output of Nyquist filter 112 would require 10 bit by 10 bit multiplication, and this substantial 10 increase in numerical processing leads to an increase in die area to perform the transmit pre-equalization. Consequently, there is a need to provide practical implementations of a pre-equalizer in a cable modem without substantially increasing die area.

### Brief Description of the Drawings

Fig. 1 is a functional diagram of a cable modem.

15 Fig. 2 is a Nyquist filter.

Fig. 3 is a flow diagram for obtaining the in-phase and quadrature filter coefficients of an embodiment of the invention.

Fig. 4 is a filter for Nyquist filtering and pre-equalization according to an embodiment of the invention to obtain in-phase components.

20 Fig. 5 is a filter for Nyquist filtering and pre-equalization according to an embodiment of the invention to obtain quadrature components.

Fig. 6 is another filter structure for a sub-block of the filter in Fig. 5.

Fig. 7 illustrates a computer system employing an embodiment of the present invention.

### 25 Description of Embodiments

Embodiments according to the present invention provide efficient pre-equalization by combining a pre-equalizer with a Nyquist filter. Combining pre-equalization with Nyquist filtering results in a filter structure having no more inherent complexity than a Nyquist filter by itself. In particular, the numerical computations 30 involved in filter weight multiplication are no more involved than performing Nyquist filtering by itself.

A flow diagram illustrating the synthesis of the combined filter is provided in Fig. 3. For box 302 a pre-equalizer is synthesized as an FIR filter having impulse response (filter weights)  $g(i) = g_I(i) + jg_Q(i), i = 0, 1, \dots, L-1$ , where  $g_I(i)$  are the in-phase components of the filter weights  $g(i)$  and  $g_Q(i)$  are the quadrature components of the filter weights  $g(i)$ . This synthesis may be accomplished by any well-known technique, such as measuring the impulse response of the cable channel and equalizing accordingly.

For box 304, given the Nyquist filter impulse response  $c(i), i = 0, 1, \dots, N-1$ , the combined filter, denoted as  $c'(i) = c'_I(i) + jc'_Q(i), i = 0, 1, \dots, N+L-2$ , is given by

$$c' = g * c, \text{ where } * \text{ denotes convolution. That is, } c'(i) = \sum_{k=0}^{L-1} g(k)c(i-k), \text{ where it is}$$

understood that  $c(i) = 0$  for  $i < 0$  or  $i > N-1$ . For the embodiment of Fig. 3, the  $c(i)$  are real-valued, so that  $c'_I = g_I * c$  and  $c'_Q = g_Q * c$ .

The embodiment of Fig. 4 may be employed to obtain the in-phase components for Nyquist and pre-equalized filtered output data in which the combined filter weights are given as indicated in the flow diagram of Fig. 3. Similarly, the embodiment of Fig. 5 may be employed to obtain the quadrature component for the output data.

The in-phase and quadrature components of the input discrete-time signal to the filters of Figs. 4 and 5 are each 2 bits. Multipliers 406 and 506 in Figs. 4 and 5 need only perform 2 bit by J bit multiplication, where J is the word length of the filtered output in bits. For example, in one embodiment, the in-phase and quadrature inputs to modulator 114 are 10 bits, so that the filter weights in Figs. 4 and 5 are 10 bits and multipliers 406 and 506 perform 2 bit by 10 bit multiplication. Multiplication by a 2 bit number is relatively easy to implement in hardware, requiring only a bit shift followed by addition. Note that if Nyquist filtering and pre-equalization are not combined as described in Fig. 3, but instead pre-equalization is performed after Nyquist filtering, then providing 10 bit outputs would require 10 bit by 10 bit multiplication, which is more costly than simple 2 bit by 10 bit multiplication.

As described before, interpolation elements 404 and 504 in Fig. 4 and 5 insert three zeros for each received sample of the input discrete-time signal, so that the resulting filtered output is provided at four times the data rate as the input to the filter. Adders 402

and **502** in Figs. 4 and 5 add the resulting 10 bit numbers from multipliers **406** and **506** to provide the filtered output. Adders **402** and **502** also round the resulting addition, so that the final output has  $J$  bit word length, where in one embodiment,  $J = 10$ .

Various other known filter structures may be employed to perform combined

5 Nyquist filtering and pre-equalization. For example, Fig. 6 is an alternative filter implementation for sub-block **406** of Fig. 4, where in Fig. 6  $N' = N - L - 1$ . Filters similar in structure to that of Fig. 6 may also be used for other sub-blocks (not shown) in Figs. 4 and 5. The filter structure of Fig. 6 has several advantages over that of Fig. 4.

10 Multipliers **602** in Fig. 6 operate at the input data rate, whereas multipliers **406** in Fig. 4 operate at four times the input data rate. Similarly, adders **604** operate at the input data rate. Multiplexer **606**, however, operates at four times the input data rate, and multiplexes the output of sub-blocks **608** to provide an output signal at four times the input data rate. Because of round-off errors, the filter of Fig. 6 will often not be numerically identical to that of Fig. 4. Another important advantage of the filter in Fig. 6 is the savings in delay 15 elements **610**. The filter in Fig. 6 has approximately one-fourth as many delay elements as sub-block **406** in Fig. 4. Many other well-known filter structures may be utilized to perform the filtering indicated in Fig. 4, although the final filtered output may not be identical to that of Fig. 4 due to round off error.

20 Embodiments of the present invention may be employed in many devices and systems. One such system is illustrated in Fig. 7, where computer system **702** comprises central processing unit (CPU) **704**, chipset **706**, system memory **708**, and system bus **710**. Modem **712** is coupled to a cable (not shown) through cable interface **118**, and is coupled to system bus **710** to communicate with CPU **704**.

25 Clearly, various modifications may be made to the disclosed embodiments without departing from the scope of the invention as claimed below.